1. A method of forming a metal oxide semiconductor field effect transistor (MOSFET) on a semiconductor substrate, comprising the steps of:

providing a gate insulator layer, and an overlying conductive layer on said semiconductor substrate;

forming a mask shape on said conductive layer;

performing a first dry etch procedure using said mask shape to form a tapered conductive gate structure on said gate insulator layer with top surface of said conductive gate structure comprised with a smaller width than a bottom surface of said tapered conductive gate structure;

performing an ion implantation procedure to form a lightly doped source/drain (LDD) region in an area of said semiconductor substrate not covered by said tapered conductive gate structure, and to implant ions into portions of said tapered conductive gate structure, through tapered sides of said tapered conductive gate structure;

performing a second dry etch procedure to remove portions of said tapered conductive gate structure comprised with said implanted ions resulting in a straight walled conductive gate structure, and resulting in said LDD region offset from edges of said straight walled conductive gate structure;

forming sidewall spacers on said straight walled conductive gate structure; and

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said straight walled conductive gate structure of by said sidewall spacers.

2. The method of claim 1, wherein said MOSFET device is an N channel (NMOS) device.

3. The method of claim 1, wherein said MOSFET device is a P channel (PMOS) device.

4. The method of claim 1, wherein said conductive layer is a doped polysilicon layer.

5. The method of claim 1, wherein said mask shape is comprised of silicon nitride.

6. The method of claim 1, wherein said mask shape is comprised of silicon oxynitride.

7. The method of claim 1, wherein said mask shape is comprised of silicon oxide.

8. The method of claim 1, wherein said first dry etch procedure is a reactive ion etch (RIE) procedure, performed at a power between about 300 to 800 watts, at a pressure between about 5 to 80 mtorr, using Cl_2, HBr, O_2, CF_4 and He as an etchant for said conductive layer.

9. The method of claim 1, wherein the width of the bottom of said tapered conductive gate structure is between about 100 to 200 Angstroms larger than the width of the top of said tapered conductive gate structure.

10. The method of claim 1, wherein said ion implantation procedure is performed using arsenic or phosphorous ions at an energy between about 3 to 10 KeV, at a dose between about 1E12 to 1E14 atoms/cm^2.

11. The method of claim 1, wherein said second dry etch procedure is a RIE procedure performed at a power between about 800 to 1000 watts, and at a pressure between about 50 to 100 mtorr, using Cl_2, HBr, O_2, and N_2 as etchants.

12. The method of claim 1, wherein said offset of said LDD region from edges of said straight walled conductive gate structure is between about 50 to 100 Angstroms.

13. The method of claim 1, wherein said sidewall spacers on said straight walled conductive gate structure are comprised of either silicon oxide or silicon nitride, at a thickness between about 200 to 800 Angstroms.

14. The method of claim 1, wherein said heavily doped source/drain region is formed via implantation of arsenic or phosphorous ions, performed at an energy between about 30 to 100 KeV, at a dose between about 1E15 to 1E16atoms/cm^2.

15. A method of forming a MOSFET device on a semiconductor substrate featuring an LDD region offset from a portion of said semiconductor substrate located underlying the edges of a polysilicon gate structure, comprising the steps of:

forming an gate insulator layer on said semiconductor substrate;

forming a polysilicon layer on said gate insulator layer;

forming a mask layer on said polysilicon layer;

performing a first dry etch procedure to define a mask shape from said mask layer;

performing a second dry etch procedure using said mask shape as an etch mask to define a polysilicon gate structure from said polysilicon layer, wherein said polysilicon gate structure is comprised with a top portion featuring vertical sides, and comprised with a bottom portion featuring notches or voids at polysilicon - silicon dioxide gate insulator layer interface, with said notches in said bottom portion of said polysilicon gate structure exposing a first portion of said semiconductor substrate while non- notched area of said bottom portion of said polysilicon gate structure is located overlying a second portion of said semiconductor substrate;

performing a first ion implantation procedure to form said LDD region in a third portion of said semiconductor substrate, wherein said third portion of said semiconductor substrate is not overlaid by said top portion of said polysilicon gate structure;

removing said mask shape;

forming insulator spacers on sides of said polysilicon gate structure filling said voids at said polysilicon - gate insulator layer interface; and

performing a second ion implantation procedure to form a heavily doped source/drain region in a area of said semiconductor substrate not covered by said polysilicon gate structure or by said insulator spacers.

16. The method of claim 15, wherein said MOSFET device is an N channel (NMOS) device.

17. The method of claim 15, wherein said MOSFET device is a P channel (PMOS) device.

18. The method of claim 15, wherein said gate insulator layer is obtained via thermal oxidation procedures to a thickness between about 10 to 80 Angstroms.

19. The method of claim 15, wherein said polysilicon layer is a doped polysilicon layer, obtained via LPCVD procedures at a thickness between about 800 to 2000 Angstroms, and wherein said polysilicon layer is in situ doped during deposition via the addition of arsine or phosphine to a silane or to a disilane ambient.

20. The method of claim 15, wherein said mask layer is a silicon nitride layer obtained via LPCVD or via PECVD procedures at a thickness between about 200 to 800 Angstroms.

21. The method of claim 15, wherein said first dry etch procedure used to form said mask shape, is an anisotropic RIE procedure performed using either CF_4, C_4F_8, CHF_3 or CH_2F_2 as an etchant.

22. The method of claim 15, wherein said second dry etch procedure used to define said polysilicon gate structure, is an RIE procedure performed at a power between about 300 to 900 watts, at a pressure between about 5 to 80 mtorr, using an etch chemistry comprised of Cl_2, HBr, O_2, CF_4, N_2 and He.

23. The method of claim 15, wherein said notches located in said bottom portion of said polysilicon gate structure, extend inwards between about 150 to 200 Angstroms from the vertical sides of said top portion of said polysilicon gate structure.

24. The method of claim 15, wherein said first ion implantation procedure used to form said LDD region, is performed using arsenic or phosphorous ions at an energy between about 3 to 10 KeV, at a dose between about 1E12 to 1E14 atoms/cm^2, and at an implant angle of 0 degrees.

25. The method of claim 15, wherein said mask shape is removed using a hot phosphoric acid solution.

26. The method of claim 15, wherein said insulator spacers on sides of said polysilicon gate structure are comprised of either silicon oxide or silicon nitride, at a thickness between about 200 to 800 Angstroms.

27. The method of claim 15, wherein said second ion implantation procedure used to form said heavily doped source/drain region is performed using arsenic or phosphorous ions, at an energy between about 30 to 100 KeV, at a dose between about 1E15 to 1E16 atoms/cm^2.